IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

Appl. No.:10/099,680

Applicant(s): FRANK W. ROHLFING

Filed: March 15, 2002

Title: ELECTRONIC DEVICES COMPRISING THIN-FILM TRANSISTORS AND THEIR MANUFACTURE

TC/A.U.: 2800/2813

Examiner: L.M. Schillinger

Atty. Docket: GB 010043

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On: 12 January 2005

By: Michelle Welgoss

Michelle Welgoss

REPLY BRIEF

Mail Stop- APPEAL BRIEF
Honorable Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Examiner's Answer (hereafter, the Answer) dated November 12, 2004, Applicant provides the following Reply Brief in the above captioned application.

It is noted that the Real Party in Interest was erroneously listed as U.S. Philips Corporation in the Appeal Bried. In preparing this Reply Brief, this error was discovered. The real party as assignee of the entire right and title to the invention interest is: Koninklijke Philips Electronics, N.V. having an address of Groenenwoudseweg 1, NL-

5621 BA Eindhoven, NL. The undersigned greatly regrets any inconvenience.

Although Applicant generally affirms all arguments previously presented in his Appeal Brief, for brevity, Applicant respectfully address the rebuttal arguments presented in the Answer.

Argument

Claims 1-11 are patentable over *Bae*

1. The Examiner Improperly Attempts to Construe One Method Step of *Bae* into Two Steps of the Claimed Method

i.) At page 3 of the Answer, the Examiner asserts that Bae teaches:

> "b) depositing a first mask over the semiconductor film and forming holes therethrough (Fig. 3B (100 and 54a));
> c) patterning the mask in a first pattern (Fig. 3B (100 and 54a)-note that layer 100 is referred to as a photoresist pattern and such patterning occurs due to patterned light exposure in the formation of the resist);"

In the description surrounding Figs. 3A and 3C, *Bae* discloses the formation of a refractory metal layer 54 and an oxide layer 55. *Bae* then discloses that next photolithographic processing is performed "...using a resist pattern to etch the refractory metal layer 54 and the oxide layer 55 except the portions positioned over the channel region of the MOS transistor , until the partial top surface of the gate polysilicon 53 are exposed. Thereby a gate metal layer 54a and a buffering layer 55a are formed as shown in Fig. 3B." As

described in connection with Fig. 3C, the gate metal layer 54a and buffering layer 55a serve as a mask in the implantation of N-type or P-type impurities. (Kindly refer to column 4, lines 12-44 as well as Figs. 3A-3C of the reference to *Bae*.)

Clearly, from the referenced portion of *Bae*, there is a standard photoresist deposition, patterning and etching sequence to form a mask of layers 54a and 55b. However, there is no teaching or suggestion that in addition, **holes are formed in the mask**. In furtherance of this assertion, it is noted that the reference to *Bae* may disclose a technique by which a mask is formed of components of a gate structure (namely gate metal layer 54a and buffering layer 55b), but does not disclose *depositing a first masking layer over the semiconductor film and removing portions thereof to form* ***a plurality of holes*** as featured in claim 1.

The Examiner attempts to cure the noted deficiency of *Bae* by asserting that the featured plurality of holes is met by the patterning and etching sequence disclosed in *Bae* to realize the mask formed by layers 54a and 55a. However, by doing so, the Examiner is attempting to meet **two separate processing steps of claim 1** with the disclosure of only **one processing step** described in *Bae*. This is wholly improper. To wit, the etching sequence of *Bae* may be germane to the step of "*...patterning the first masking layer in a first pattern...*" as recited in claim 1. However, it is entirely improper to apply one and the same processing step in *Bae* to the **additional** step of claim 1: "*...depositing a first masking layer over the semiconductor film and removing portions thereof to form* ***a plurality of holes...***"

For at least the reasons set forth above, it is respectfully submitted that the reference to *Bae* lacks at least one feature of claim 1. For at least this reason, claim 1 and the claims that depend therefrom are patentable over the applied art. Allowance is earnestly solicited.

ii.) In the Answer, the Office asserts that "The Examiner has interpreted the term "hole" under its broadest reasonable interpretation in light of the specification and determined that upon the semiconductor substrate, it is understood that there are a plurality of gate structures 54a and 55b formed on the substrate and they are separated by an etching layer 54a and 55b. This removal step is consistent with the definition of "hole" referred to in the dictionary and relied upon by the Applicant. Therefore, the Examiner does not find the argument persuasive that the *Bae* reference does not teach forming a plurality of holes as stated by the arguments." (Kindly refer to page 5 of the Answer.)

Applicant respectfully traverses to the above assertions.

First, Applicant respectfully requests clarification as to certain points. In particular, the Answer asserts that Bae discloses "...a plurality of gate structures 54a and 55b formed on the substrate and they are separated by an etching of holes in layer 54a and 55a..." Applicant respectfully questions how the gate structures 54a and 55b can be formed on the substrate and be separated by holes in themselves? Clarification is respectfully requested. Moreover, the opportunity to respond after this position is clarified is believed to be of-right since a meaningful response is not possible at present due to the lack of clarity of the assertion.

The above request for clarification notwithstanding, Applicant respectfully submits that *Bae* does not disclose the etching of holes in the layers 54a and 55a as the Examiner asserts.

Second, it is noted that the Examiner has articulated a clear distinction between the reference to Bae and the features of claim 1. In attempting to cure the deficiencies of *Bae*, the Examiner asserts that the reference to *Bae* **discloses forming a plurality of gate structures 54a and 55a**. Moreover, the Examiner notes that layers 54a and 55a are used as masks. (Kindly refer to pages 4 and 5 of the Answer.) However, the forming of a plurality of implant masks does not equate to the features of claim 1, which includes *depositing a* ***first masking layer*** *over the semiconductor film and* ***removing portions thereof to form a plurality of holes***. It is respectfully submitted that the Examiner is attempting to maintain the unreasonable and improper position that a plurality of implant masks as set forth in *Bae* is the same as forming a plurality of holes in one masking layer, as set forth in the noted step of claim 1 of the present application.

For at least the reasons set forth above, it is respectfully submitted that the rejection in view of *Bae* lacks is improper. For at least this reason, claim 1 and the claims that depend therefrom are patentable over the applied art. Allowance is earnestly solicited.

2. The Examiner Attempts to Require More Than One Implantation Step in Contradistinction to the Written Description

2. In the Answer, the Examiner asserts that the feature of claim 1, *performing* ***an implantation*** *in the semiconductor film* includes one or more implantation because Applicant has not specifically claimed "only one ion implantation" and because claim 1 includes the transitional term 'comprising' after the preamble of the claim. The Office then recites certain court opinions germane to the transitional term 'comprising.'

However, the Examiner has failed to reconcile the above-assertions with the holdings of *KCJ Corp. v. Kinetic Concepts* and *Abtox Inc. v. Exitron Corp.*, which were cited and discussed in the Brief on Appeal. In particular, while it is generally the case that the use of an indefinite article (e.g., 'a' or 'an') in a claim having the transitional term 'comprising' is interpreted to mean 'one or more' of this element, an exception exists and applies in the present application. In particular, an exception exists when "The written description supplied additional context for understanding whether the claim language limits the patent scope to a single unitary [element] or extends to encompass a device with multiple [elements]." *KCJ Corp. v. Kinetic Concepts Inc.* 55 USPQ 2d 1835, 1839, citing *AbTox, Inc. v. American Cyanamid Co.* 28 USPQ 2d 1545. The CAFC further states in *KCJ Corp.* "Thus, as the rule dictates, when the claim language or context calls for further inquiry, this court consults the written description for a clear intent to limit the invention to a singular embodiment." *Id.*, at 1839.

Claim 1 features:

(f) performing **an implantation** in the semiconductor film using at least the first masking layer as an implantation mask **to define source and drain regions, an undoped conduction channel between the source and drain regions, and a field-relief region** having a lower doping concentration than the drain region between the conduction channel and the drain region.

Clearly, claim 1 envisions a single implantation step for the forming of the source and drain, the undoped channel and a field relief region. The filed application describes clearly the use of a single implantation step. For example, the specification states:

> "It is desirable to fabricate the source, drain and the field relief region in a single implantation step in order to simplify the TFT manufacturing process, which will reduce produce production costs and improve throughput and yield." (page 2, lines 18-22 of the filed application);
>
> "It is an aim of the present invention to provide an improved method of defining field relief regions in a single implantation step" (page 2, lines 28-29 of the filed application);
>
> "Combined implantation of source, drain and field relief regions can thus be achieved with the use of a masking layer or template..." (page 3, lines 16-18 of the filed application); and
>
> "The spacers are then removed and implantation of the semiconductor film 2 is carried out, with the exposed portions of perforated insulating layer 8 constituting a first, partial mask, and the gate layer 10 acting as a second mask. This results in the definition of the source 16 and drain 18, field relief regions 20, 22 and a conduction channel 24 in the semiconductor film 2." (page 7, lines 21-25 of the filed application. See also Figs. 1b and 1c.)

From the written description of the filed application it can be appreciated that **a clear aim and benefit of the**

processes disclosed in the filed application is the fabrication of the source, drain, field-relief regions, and the channel in a **single implantation**, and not the multiple implants that are required by and plague known techniques, and as are required by *Bae*. Thus, it is respectfully submitted that ***one and only one*** implantation is desired and one and ***only one implantation*** is described in the filed application. Accordingly, Applicant respectfully submits that the written description supplies additional context for understanding that the claim language limits the patent scope to a single implantation and does not extend to encompass multiple implantations. Therefore, following *KCJ Corp. v. Kinetic Concepts Inc.* and *AbTox, Inc. v. American Cyanamid Co.* it is respectfully submitted that the feature of claim 1, '*performing* ***an implantation***,' means performing only one implantation.

For at least the reasons set forth in the Appeal Brief and the reasons set forth above, Applicant reiterates his position that independent claim 1 and the claims that depend directly or indirectly therefrom are patentable over the applied art.

Conclusion

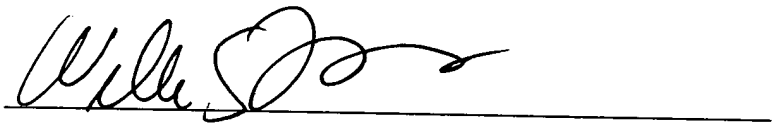
In view of the foregoing, applicant(s) respectfully request(s): the withdrawal of all objections and rejections of record; the allowance of all the pending claims; and the holding of the application in condition for allowance.

If any points remain in issue that may be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17, **or under 37 C.F.R. §41.20.**

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

Respectfully submitted on behalf of:
U.S. Philips Corporation



by: William S. Francos (Reg. No. 38,456)
date: January 12, 2005

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